

The diagram illustrates a memory array 100 with two word lines, WL1 (word line) and WL2 (word line), and six bit lines: BL1a (drain), BL2a (drain), BL3a (drain), BL1b (source), BL2b (source), and BL3b (source). A dashed circle highlights a memory cell M1 at the intersection of WL1 and BL2a. The circuit shows access transistors and storage capacitors for each cell.

Fig. 2

	BL1a	BL1b	BL2a	BL2b	BL3a	BL3b	WL1	WL2
Erase	F	F	F	F	F	F	-Vpp	0
Write	Vppx	F	0	F	Vppx	F	Vpp	<Vppx
Read	Vr	0	Vr	0	Vr	0	~Vcc	0

Fig. 2a

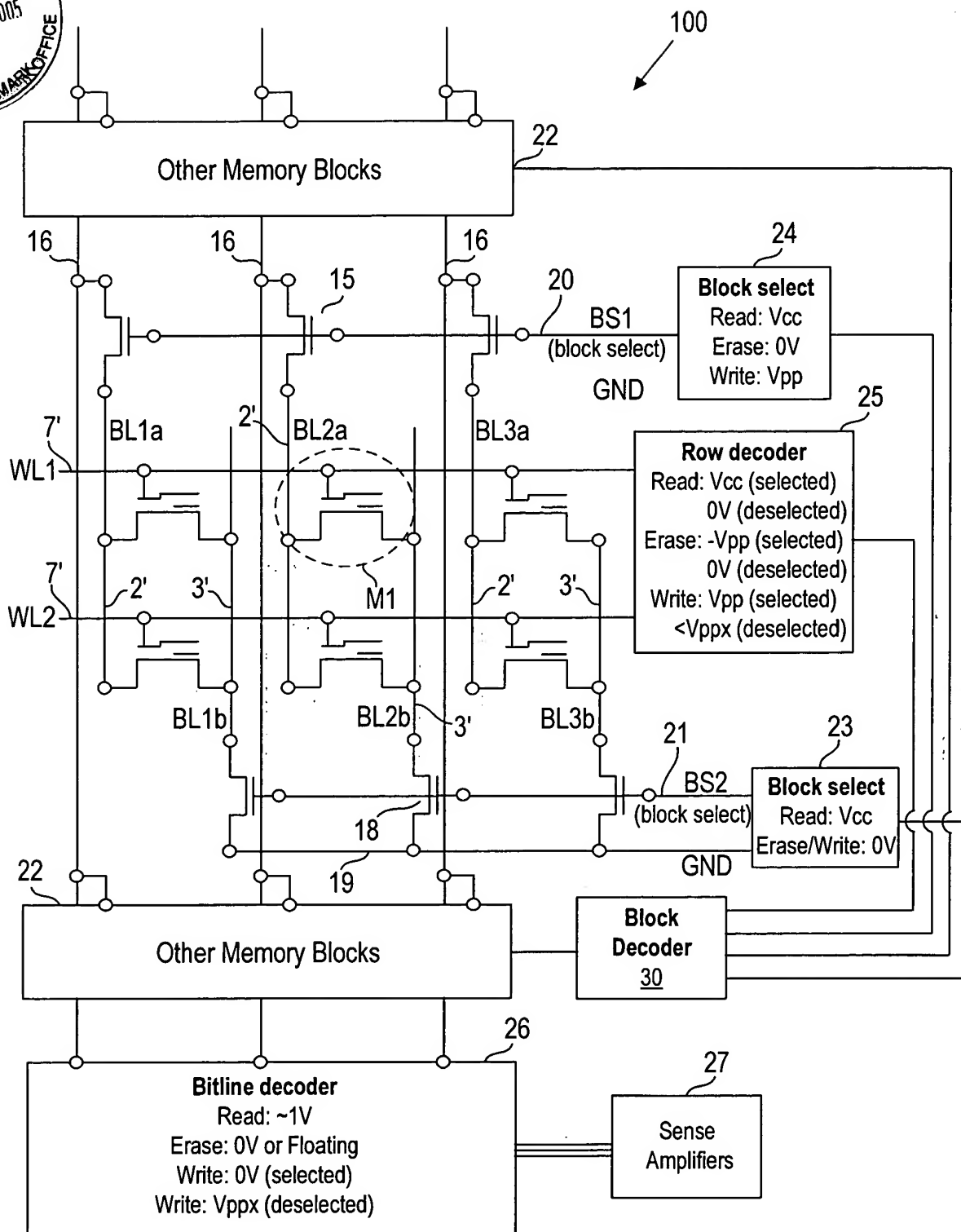


Fig. 3



Fig. 4a

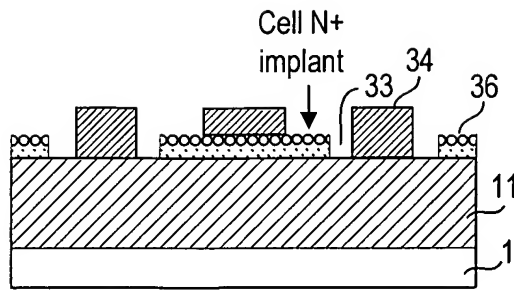


Fig. 4b

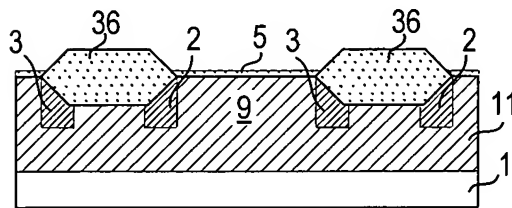


Fig. 4c

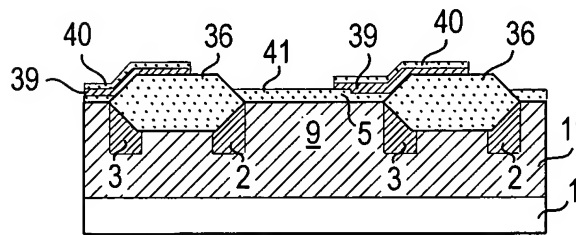


Fig. 4d

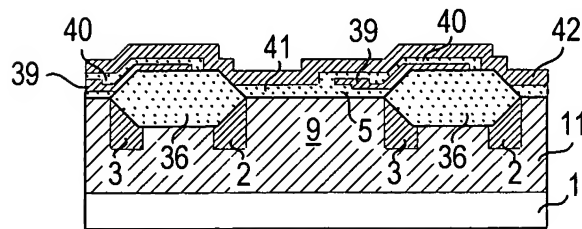


Fig. 4e

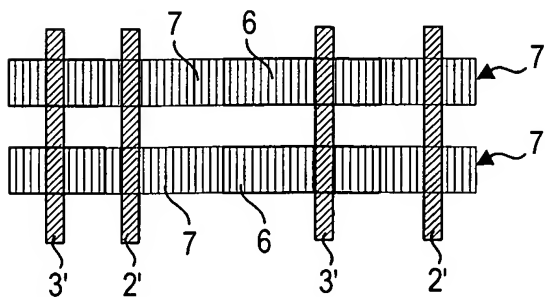




Fig. 5a

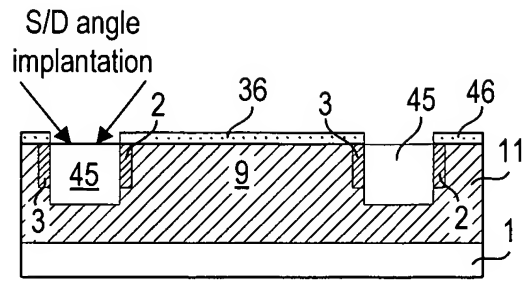


Fig. 5b

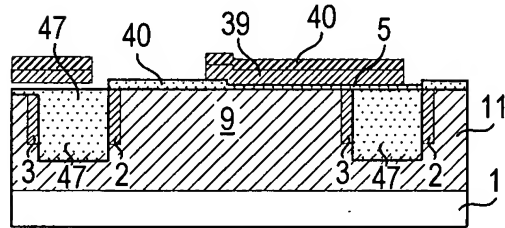


Fig. 5c

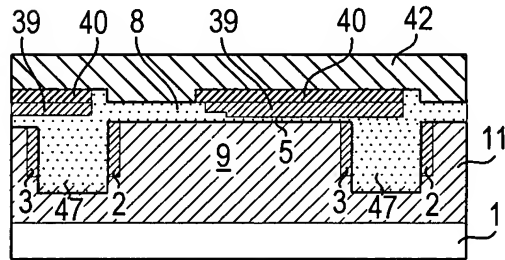
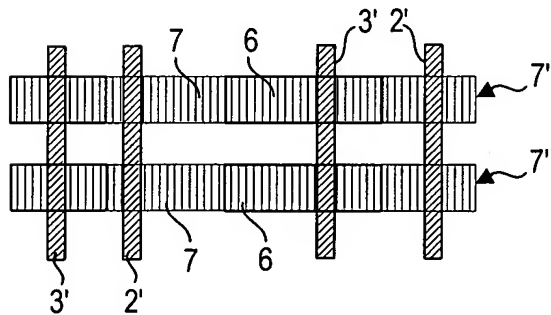


Fig. 5d





	BL1a	BL1b	BL2a	BL2b	BL3a	BL3b	WL1	WL2	Pwell	Nwell
Erase	F	F	F	F	F	F	0	Vpp	Vpp	Vpp
Write	Vppx	F	0	F	Vppx	F	Vpp	<Vppx	0	0
Read	Vr	0	Vr	0	Vr	0	~Vcc	0	0	0

Fig. 7a

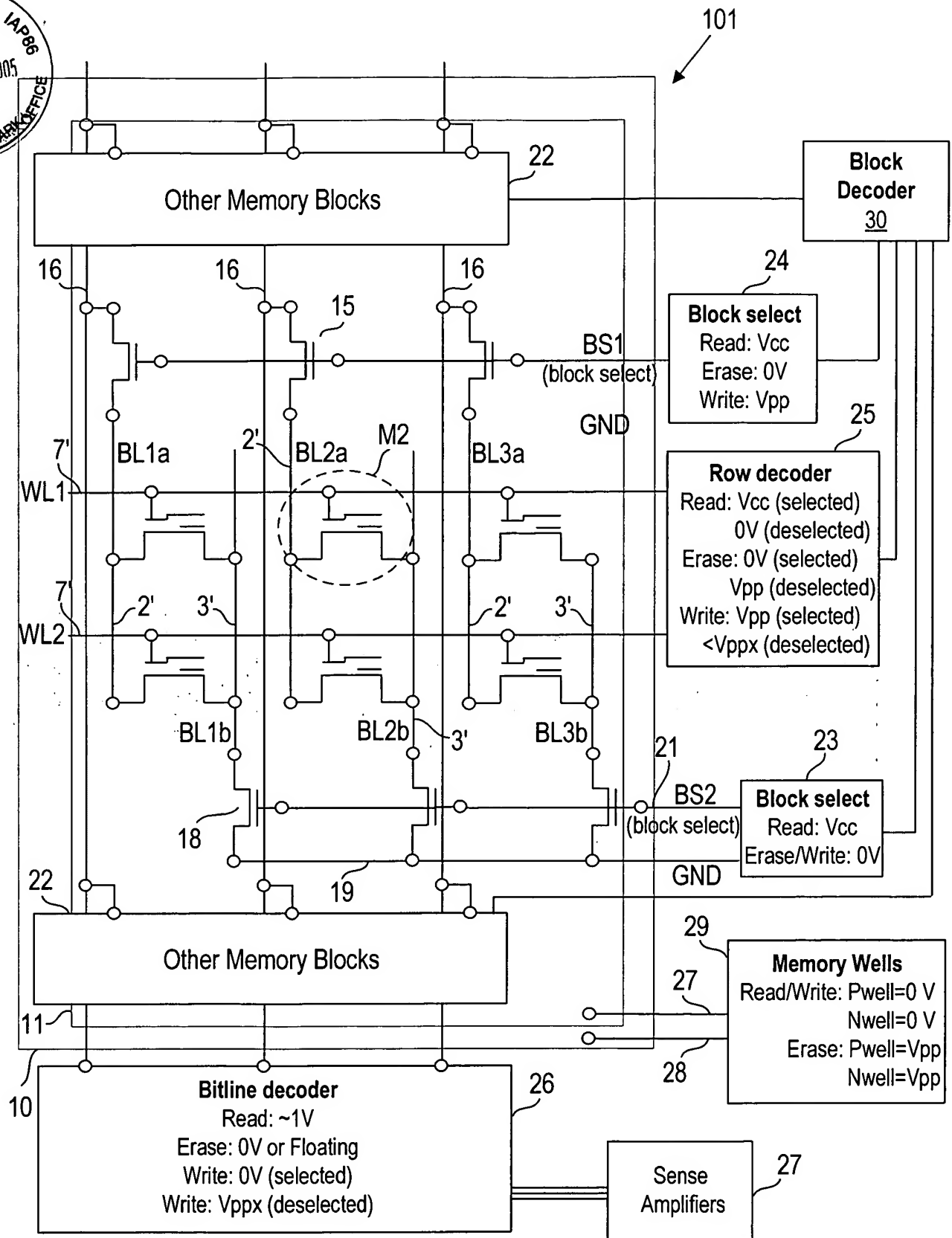
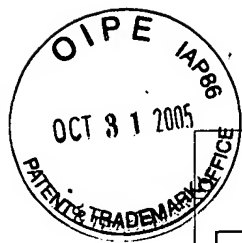


Fig. 8



Fig. 9a

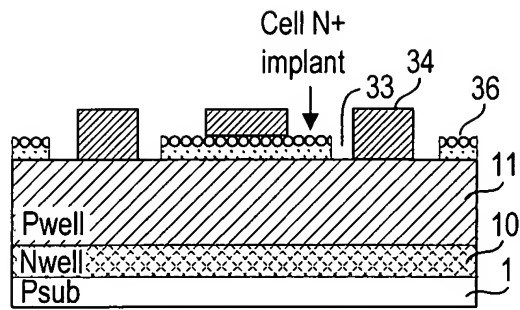


Fig. 9b

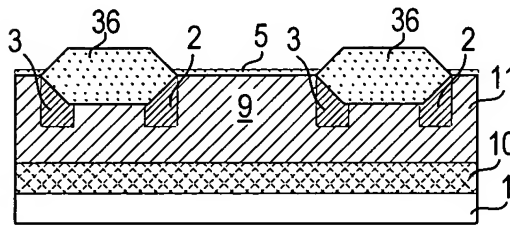


Fig. 9c

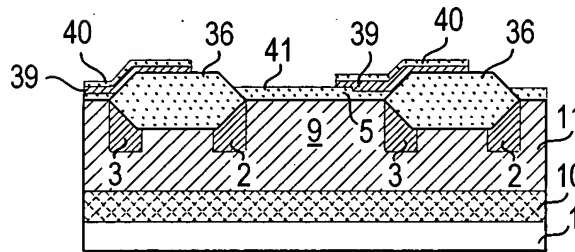


Fig. 9d

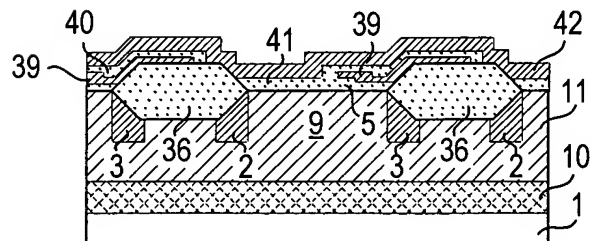


Fig. 9e

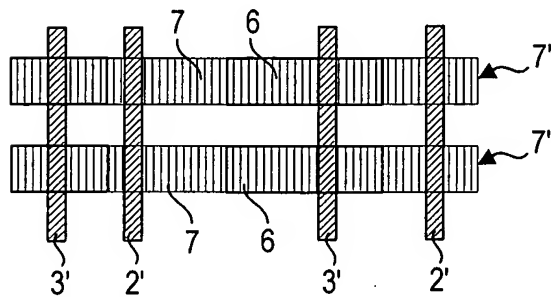




Fig. 10a

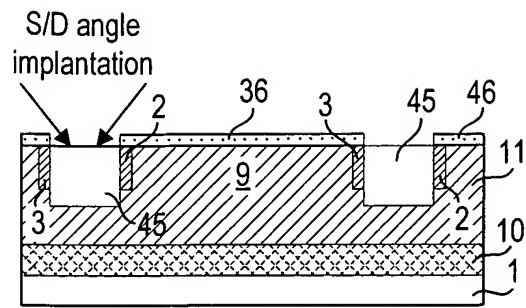


Fig. 10b

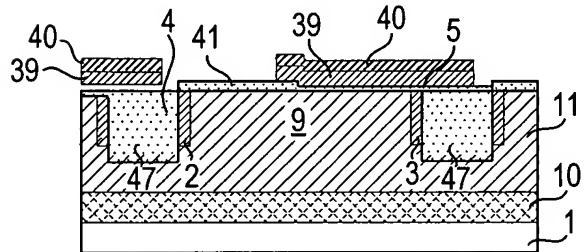


Fig. 10c

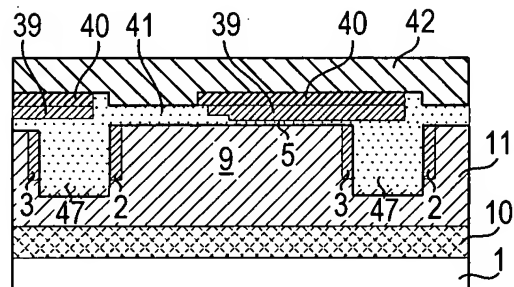


Fig. 10d

